

CLAIMS

What is claimed is:

- 1 1. An integrated circuit (IC) comprising:
2 a plurality of circuit rows, at least one row of said plurality of circuit rows
3 including three or more voltage islands;
4 at least one low voltage island in said at least one row, circuit elements in each
5 said at least one low voltage island being powered by a low voltage (V_{ddl}) supply; and
6 at least one high voltage island in said at least one row, circuit elements in each
7 said at least one high voltage island being powered by a high voltage (V_{ddh}) supply, V_{ddh}
8 being a higher voltage than V_{ddl} .
- 1 2. An IC as in claim 1 wherein said at least one low voltage island is a low voltage
2 macro.
- 1 3. An IC as in claim 1 wherein said at least one low voltage island is a low voltage
2 latch.
- 1 4. An IC as in claim 1 wherein said at least one low voltage island is a low voltage
2 cell.
- 1 5. An IC as in claim 1 wherein said at least one low voltage island spans two or
2 more of said plurality of circuit rows.
- 1 6. An IC as in claim 5 wherein said at least one low voltage island is surrounded by
2 a plurality of high voltage islands.

1 7. An IC as in claim 6 wherein said plurality of high voltage island include a high
2 voltage standard cell, a high voltage latch and a high voltage macro.

1 8. An IC as in claim 1 wherein said at least one high voltage island includes at least
2 one level converter receiving an output from said at least one low voltage island.

1 9. An IC as in claim 8 wherein said at least one low voltage island comprises a
2 plurality of low voltage islands and said at least one level converter comprises a plurality
3 of level converters in said high voltage island receiving outputs from said plurality of low
4 voltage islands.

1 10. A method of reducing power in an integrated circuit (IC) design, said method
2 comprising the steps of:

3 a) placing and wiring circuit elements for timing closure at a first supply
4 voltage;

5 b) assigning a plurality of circuit elements for replacement as low voltage
6 circuit elements in a logic aware supply voltage assignment, wherein said low voltage
7 circuit elements operate at a supply voltage below said first supply voltage;

8 c) optimizing level converter placement; and

9 d) adjusting assignment of low voltage circuit elements responsive to cell
10 placement in a physically aware voltage re-assignment.

1 11. A method as in claim 10 further comprising repeating steps (b) – (d) until no
2 circuit elements are assigned for replacement in assigning step (b) and no assignment
3 adjustment is needed in assignment adjusting step (d).

1 12. A method as in claim 11, further comprising the steps of:

2 e) placing a power grid to form placed cells in a high and low voltage
3 islands; and

4 f) passing said placed design to a physical synthesis engine.

1 13. A method as in claim 10 wherein the logic aware placement in step (b) comprises
2 the steps of:

- 3 i) identifying ones of said circuit elements with timing slack; and
4 ii) selectively replacing identified said ones with low voltage equivalent
5 circuit elements.

1 14. A method as in claim 13 wherein circuit elements include one or more macros, a
2 plurality of latches and a plurality of cells and the logic aware assignment step (b) further
3 comprises placing level converters at selected outputs of replaced said low voltage
4 macros, said low voltage latches and said low voltage cells.

1 15. A method as in claim 13 wherein the steps (ii) of selectively replacing said
2 identified ones comprises the steps of:

- 3 A) selecting a candidate from said identified ones
4 B) replacing said candidate with a low voltage equivalent circuit element;
5 C) checking a timing specification for said candidate; and
6 D) determining whether said low voltage equivalent meets said timing
7 specification.

1 16. A method as in claim 15 wherein when said low voltage equivalent fails to meet
2 said timing specification in step (D), said method further comprises reverting the replaced
3 said low voltage equivalent to said circuit element selected as said candidate.

1 17. A method as in claim 16 further comprising:

- 2 E) determining whether any candidates remain unchecked; and
3 F) selecting an unchecked said candidate and returning to step (B) until all
4 candidates are determined checked in step (E).

1 18. A method as in claim 17 wherein a plurality of said circuit elements are latches
2 and the step (D) of determining whether latch candidates meet said timing specification
3 comprises determining if all input low voltage latch input pins still have positive slack
4 and whether the output pin slack exceeds a minimum threshold.

1 19. A method as in claim 18 wherein said minimum threshold exceeds the delay for a
2 level converter.

1 20. A method as in claim 10 wherein the physically aware voltage reassignment step
2 (d) comprises determining a physical adjacency metric (PAM) for each said low voltage
3 circuit element and reverting all cells with a PAM less than a selected threshold.

1 21. A method as in claim 10 wherein an input netlist, technology definition and
2 timing constraints are provided for placing and wiring step (a).

1 22. A computer program product for integrated circuit (IC) design, said computer
2 program product comprising a computer usable medium having computer readable
3 program code thereon, said computer readable program code comprising:
4 computer program code means for placing and wiring circuit elements for timing
5 closure at a first supply voltage;
6 computer program code means for a logic aware supply voltage assignment
7 identifying and assigning a plurality of circuit elements for replacement as low voltage
8 circuit elements, wherein said low voltage circuit elements operate at a supply voltage
9 below said first supply voltage;
10 computer program code means for optimizing level converter placement; and
11 computer program code means for physically aware voltage re-assignment
12 adjusting assignment of low voltage circuit elements responsive to cell placement.

1 23. A computer program product as in claim 22, further comprising:
2 computer program code means for placing a power grid to form placed cells in a
3 high and low voltage islands; and
4 computer program code means for passing said placed design to a physical
5 synthesis engine.

1 24. A computer program product as in claim 22, wherein the computer program code
2 means for logic aware placement comprises:
3 computer program code means for identifying ones of said circuit elements with
4 timing slack; and
5 computer program code means for selectively replacing identified said ones with
6 low voltage equivalent circuit elements.

1 25. A computer program product as in claim 24, wherein circuit elements include one
2 or more macros, a plurality of latches and a plurality of cells and said computer program
3 code means for logic aware assignment step further comprises computer program code
4 means for placing level converters at selected outputs of replaced said low voltage
5 macros, said low voltage latches and said low voltage cells.

1 26. A computer program product as in claim 24 wherein said computer program code
2 means for selectively replacing said identified ones comprises:
3 computer program code means for selecting a candidate from said identified ones
4 computer program code means for replacing said candidate with a low voltage
5 equivalent circuit element;
6 computer program code means for checking a timing specification for said
7 candidate; and
8 computer program code means for determining whether said low voltage
9 equivalent meets said timing specification.

1 27. A computer program product as in claim 26 wherein said computer program code
2 means for determining when said low voltage equivalent fails to meet said timing
3 specification further comprises computer program code means for reverting replaced said
4 low voltage equivalents to said circuit elements selected as said candidates.

1 28. A computer program product as in claim 27 wherein a plurality of said circuit
2 elements are latches and said computer program code means for determining whether
3 candidates meet said timing specification comprises determining for said latches if all
4 input low voltage latch input pins still have positive slack and whether latch output pin
5 slack exceeds a minimum threshold.

1 29. A computer program product as in claim 28 wherein said minimum threshold
2 exceeds the delay for a level converter.

1 30. A computer program product as in claim 22 wherein said computer program code
2 means for physically aware voltage re-assignment comprises:
3 computer program code means for determining a physical adjacency metric
4 (PAM) for each said low voltage circuit element; and,
5 computer program code means for reverting all cells with a PAM less than a
6 selected threshold.

1 31. A computer program product as in claim 22 further comprising computer program
2 code means for receiving an input netlist, technology definition and timing constraints for
3 a design.